(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 June 2005 (23.06.2005)

PCT

(10) International Publication Number
WO 2005/057626 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number:
PCT/US2004/040698

(22) International Filing Date: 3 December 2004 (03.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/527,463 4 December 2003 (04.12.2003) US

(71) Applicant *(for all designated States except US)*: GREAT WALL SEMICONDUCTOR CORPORATION [US/US]; P.O Box 24619, Southern Avenue, Tempe, AZ 85285-4619 (US).

(72) Inventor: OKADA, David, N.; 7855 South River Parkway, Suite 122, Tempe, AZ 85284 (US).

(74) Agents: SAMUEL, Richard, I. et al.; Goodwin Procter LLP, 103 Eisenhower Parkway, Roseland, NJ 07068 (US).

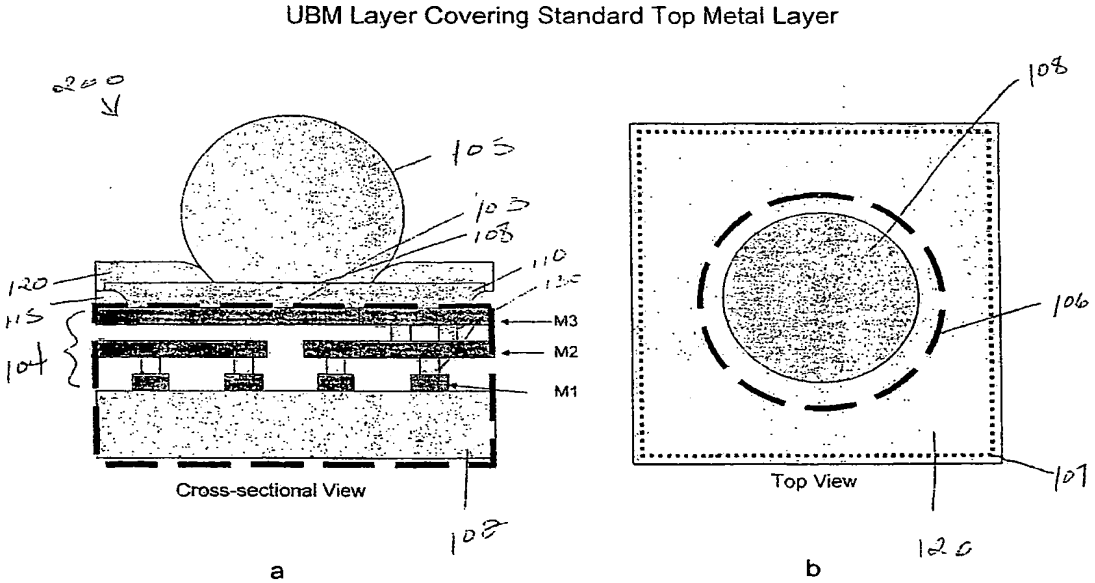
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM AND METHOD TO REDUCE METAL SERIES RESISTANCE OF BUMPED CHIP



(57) Abstract: Provided herein, in accordance with one aspect of the present invention, are exemplary embodiments of semiconductor chips having low metallization series resistance. In one embodiment, the semiconductor chip comprises a semiconductor substrate and a metallization structure formed on the semiconductor substrate; an under bump metallurgy ("UBM") structure layer formed over the metallization structure; and a bump formed over said UBM layer; wherein the largest linear dimension of said UBM layer is larger than the diameter of said bump.

WO 2005/057626 A2